REMARKS/ARGUMENTS

In response to the outstanding Office Action, the independent claims have been amended in an effort to emphasize the fact that it is the set-reset latches which provides the non-overlapping switch driver signals. In the prior art, set-reset latches and a separate successive approximation register provide set-reset latch outputs which then control non-overlapping switch drivers. Thus the non-overlapping switch drivers cannot begin to settle until the set-reset latches of the prior art settle because of the serial connection of these to functions. In the present invention, the set-reset latches themselves are configured to provide non-overlapping switch driver signals, reducing the settling time and increasing the speed of operation of the circuit.

In the outstanding Office Action, claims 1-26 were rejected under 35 USC 102(a) as being anticipated by the admitted prior art. With respect to claims 1, 12, 20 and 22, the Examiner states that "each reset latch is responsive to a combination of control signals in the output of the comparator and providing non-overlapping switch driver signals as set-reset latch outputs." This is not correct. Figure 1 clearly shows the successive approximation register having latches separate and apart from the non-overlapping switch driver. In that regard, the Examiner appears to be attempting to lump the successive approximation registers and non-overlapping switch drivers as a single element. However, this clearly is not what Figure 1 shows. The successive approximation register in Figure 1 does not provide non-overlapping switch driver signals, but separate circuits must be provided for this purpose. In the present invention, the set-reset latches in the successive approximation register, themselves, provide the non-overlapping switch driver signals, increasing the speed of operation of the circuit over that required for the ripple through of a signal in two successive circuits. This clearly distinguishes from the admitted prior art. Further, it should be noted that higher and higher speeds of operation of such circuits is always sought. Accordingly, not only is the present invention not anticipated by the admitted prior art, but it also is not rendered obvious by the admitted prior art, as if it was, set-reset latches directly providing non-overlapping switch driver output signals would have been used long ago.

With respect to claims 2-11, 13-19, 21 and 23-26, claims 8 and 16 referring to hybrid logic have been canceled, the use of the logic that may include hybrid logic being adequately covered in over claims. With respect to the terms "positive logic" and "negative logic," these terms are well defined on page 8, lines 3-7 of the present application, and accordingly, are not ambiguous. Thus, claims 2-7, 9-11, 13-15, 17-19, 21 and 23-26 are believed allowable as providing greater specificity to the claimed combinations, which overall combinations are also patentable over the prior art. With respect to the prior art made of record but not relied upon, the undersigned would like to make the following comments.

The Pilost patent discloses a non-standard search routine that yields a "rounded-off" N-bit result after N+1 comparisons. His logic implements a different search algorithm and never mentions using the outputs of the set-reset flip-flops as non-overlapping signals. In fact, he repeatedly specifies that the register output driving into the DAC is one signal per bit, so the non-overlap function must be incorporated into the DAC circuitry not discussed. There's no mention of non-overlap, break-before-make, or switch implementation in this patent.

The Somayajula patent covers an alternative way of eliminating the separate non-overlap delay by dedicating a separate D-latch and clock phase to each switch phase, i.e. each bit has more than one D-latch running off of separate clocks. This presents a very different approach to the same problem addressed by the present invention. This patent illustrates the point that eliminating the separate non-overlap circuit is a real problem that is not solved by standard prior art SAR digital paths as of a relatively late date.

The Jones patent from 1990 is a SAR implemented with superconducting loops, and is unrelated to the present invention.

CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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